REMARKS

Claims 1-58 are pending in this application. The Examiner allowed claims 38-45, rejected claims 1-13, 17, 25, 27-36, and 46-55, objected to claims 14-16, 18-24, 26, and 37, and withdrew claim 56 from consideration. Applicant appreciates the Examiner's acknowledgement of allowable subject matter, but respectfully traverses the Examiner's rejections.

Regarding the claim amendments, Applicant has amended claims 3-5, 28, 40, 46, 48, 49, and 54 to correct the apparently typographical errors of the original application. Applicant submits that these claims are amended for reasons unrelated to patentability and no new matter has been added with these Amendments. Applicant has canceled claim 56 as it is directed to a non-elected group.

Applicant has amended claim 1 to better describe Applicant's invention. The subject matter of this amendment may be found in the original application, for example, in Fig. 2 and at page 18, lines 19 though 22. Applicant has also amended claims 46 and 49 to better describe Applicant's invention. The subject matter of these amendments may be found in the original application, for example, in Fig. 2 and at page 12, line 21 though page 15, line 3. Applicant has added new claims 57 and 58, which depend from claim 1, to encompass various embodiments of Applicant's invention. The subject matter of these amendments may be found in the original application, for example, in Fig. 2 and at page 16, lines 18 though 20. No new matter has been added by these amendments.

Election/Restriction

The Examiner indicated that non-elected claim 56 was never officially canceled. Accordingly, Applicant has canceled claim 56 with this amendment. Applicant further confirms election of claims 1-55 and new claims 57 and 58 for prosecution in this application.

Drawings

The Examiner indicated that formal drawings will be required when the application is allowed. Accordingly, Applicant is submitting formal drawings concurrently with this Amendment.

Allowable Subject Matter

Dependent claims 14-16, 18-24, 26, and 37

The Examiner suggested that claims 14-16, 18-24, 26, and 37 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicant submits that these dependent claims are allowable because the claims they rely on, claims 1 and 28, are allowable at least for the reasons discussed further below. Therefore, Applicant has not amended these dependent claims in this Amendment.

Comments on Statement of Reasons for Allowance

Applicant appreciates the Examiner's acknowledgement of allowable subject matter, claims 38-45. However, Applicant respectfully objects to the Examiner's reasons for allowance regarding claim 38 because claim 38 does not contain the limitations recited by the Examiner. In particular, the Examiner provided as the reasons for allowance regarding claim 38 that "the third write data item is written to one of the two memory blocks at the initiation

of the first write burst operation[], and the fourth write data item is written to the other one of the memory blocks half a clock cycle after the initiation of the first write burst operation." (Office Action dated June 9, 2003, p. 3.) Claim 38 does not contain those limitations. Applicant respectfully requests that the Examiner acknowledges Applicant's objections. Applicant believes that claims 38-45 remain allowable and, therefore, has not amended these claims.

Claim Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 1-4, 10-13, 17, 25, 27-31, and 46-54 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,749,086 to Ryan and U.S. Patent No. 5,587,961 to Wright *et al.* ("Wright"). Applicant respectfully traverses these rejections. As is discussed further below, there is no motivation to combine or modify the teachings of Ryan with those of Wright in the manner proposed by the Examiner because Ryan's teaching suggests that such modification would defeat the intended purpose of Ryan's teachings. Additionally, even if there is a motivation to combine the teachings of Ryan and Wright as indicated by the Examiner, the combination does not teach or suggest all the limitations of independent claims 1, 28, 46, and 54, and therefore does not teach all the elements of the pending claims.

I. The Combination of Ryan and Wright does not teach or suggest all of the limitations of claims 1, 28, 46, and 54

Neither Ryan nor Wright teaches or suggests at least that "the data bus is capable of receiving data corresponding to the write burst operation and providing data corresponding to

the read burst operation with no dead cycles therebetween," as recited in claim 1. Indeed, both Ryan and Wright teach away from claim 1.

Ryan relates to memory devices in which "[n]ovel command signals CMND0 and CMND1 are supplied in place of the well known WE and OE command signals." (Ryan, Abstract.) Ryan describes "a Write Burst followed by a Read Burst" with "a Write mode" selected at "RAS time T0" and "a Switch to Read mode" initiated at "time T7." (Ryan, col. 9, ll. 62-65; col. 10, ll. 1-4.) Fig. 19 shows that the time difference between the read and write bursts is seven clock cycles. Fig. 19 also shows that there are three dead clock cycles, T7, T8, and T9, between the write operation and the read operation. Specifically, "[f]ollowing the read latency period, the first of a burst of four output data elements DOUT n is made available on the data bus 130 at time T10" and "the remaining output data is made available on the data bus, completing the Read Burst with output data DOUT n+3 at time T13." (*Id.* col. 10, ll. 6-11.). Therefore, Ryan fails to teach or suggest at least that "the data bus is capable of receiving data corresponding to the write burst operation and providing data corresponding to the read burst operation with no dead cycles therebetween," as recited in claim 1. In fact, Ryan teaches away from claim 1 by teaching the use of the "read latency period" and "one clock cycle external write latency." (*Id.* col. 10, ll. 6-8, 46-48.) Under this teaching, dead cycles are created between or within the read and write burst operations.

Wright does not cure the defects in the teachings of Ryan. Wright describes"[a] synchronous random access memory" programmed with a read latency of three or more." (Wright, Abstract.) Wright also describes that "the READ command is issued at time T1 immediately after the WRITE command issued at time T0." (Wright, col. 11, ll. 38-39.) Specifically, "[b]ecause of the read latency of three, the first output data set (DOUT b)

[initiated by the READ command issued at time T1] is provided at time T4." (*Id.* ll. 37-40.) Fig. 7 shows that there are two dead clock cycles, T2 and T3, between the write operation and the read operation. Therefore, Wright also fails to teach or suggest at least that "the data bus is capable of receiving data corresponding to the write burst operation and providing data corresponding to the read burst operation with no dead cycles therebetween," as recited in claim 1. In fact, Wright teaches away from claim 1 by teaching the use of "a read latency of three" or "greater than three." (*Id.* col. 11, ll. 30, 45.) Under this teaching, dead cycles are created between or within the read and write burst operations.

Neither Ryan nor Wright teaches or suggests "(A) initiating a first write burst operation for sequentially transferring at least a first and second write data items to the memory circuit in a first clock cycle; and (B) initiating a first read burst operation for sequentially transferring at least a first and second read data items from the memory circuit in a second clock cycle, wherein the first and second clock cycles are two consecutive clock cycles," as recited in claim 28. Indeed, both Ryan and Wright teach away from claim 28.

Ryan describes "a Write Burst followed by a Read Burst," with "a Write mode" selected at "RAS time T0" and "a Switch to Read mode" initiated at "time T7." (*Id.* col. 9, ll. 62-65; col. 10, ll. 1-4.) Fig. 19 shows that the time difference between the read and write bursts is seven clock cycles. The data transfers initiated by the read and write bursts is ended by "completing the Read Burst with output data DOUT n+3 at time T13." (*Id.* col. 10, ll. 9-11.) Fig. 19 shows that a complete data input and output process in Ryan requires a total time of fourteen clock cycles. Therefore, Ryan fails to teach or suggest "(A) initiating a first write burst operation for sequentially transferring at least a first and second write data items to the memory circuit in a first clock cycle; and (B) initiating a first read burst operation for

sequentially transferring at least a first and second read data items from the memory circuit in a second clock cycle, wherein the first and second clock cycles are two consecutive clock cycles," as recited in claim 28.

In fact, Ryan teaches away from claim 28 by teaching the use of the "read latency period" and "one clock cycle external write latency." (*Id.* col. 10, ll. 6-8, 46-48.) Under this teaching, the number of clock cycles needed to complete the data transfers is increased.

Wright does not cure the defects in the teachings of Ryan. Wright describes that "the READ command is issued at time T1 immediately after the WRITE command issued at time T0." (*Id.* col. 11, ll. 38-39.) Fig. 7 shows that the data transfers do not complete until T5 "with a read latency of three." (*Id.* ll. 30.) Fig. 7 also shows that a complete data input and output process requires a total time of five clock cycles. Therefore, Wright also fails to teach or suggest "(A) initiating a first write burst operation for sequentially transferring at least a first and second write data items to the memory circuit in a first clock cycle; and (B) initiating a first read burst operation for sequentially transferring at least a first and second read data items from the memory circuit in a second clock cycle, wherein the first and second clock cycles are two consecutive clock cycles," as recited in claim 28.

In fact, Wright teaches away from claim 28 by teaching the use of "a read latency of three" or "greater than three." (*Id.* col. 11, ll. 30, 45.) Under this teaching, the number of clock cycles needed to complete the data transfers is increased. Because both the teachings of Ryan and Wright extend the number of clock cycles needed to complete the data transfers, both Ryan and Wright teach away from claim 28.

Neither Ryan nor Wright teaches or suggests at least that "each of the first and second read data items initiated by the first read operation is read in one clock cycle, and reading the

first read data item overlaps with reading the second read data item," as recited in claim 46. In particular, Ryan describes that "[f]ollowing the read latency period, the first of a burst of four output data elements DOUT n is made available on the data bus 130 at time T10" and "the remaining output data is made available on the data bus, completing the Read Burst with output data DOUT n+3 at time T13." (Ryan, col. 10, ll. 6-11; Fig. 19.) Fig. 19 of Ryan shows that reading each data element in Ryan takes one clock cycle, and reading one data element does not overlap with reading another data item in any way. Therefore, Ryan fails to teach or suggest at least that "each of the first and second read data items initiated by the first read operation is read in one clock cycle, and reading the first read data item overlaps with reading the second read data item," as recited in claim 46.

Wright does not cure the defects in the teachings of Ryan. Wright teaches the use of "a read latency of three" or "greater than three." (Wright, col. 11, ll. 30, 45; Fig. 7.) Fig. 7 of Wright shows that reading each data element takes one clock cycle, and reading one data element does not overlap with reading another data item in any way. Therefore, Wright likewise fails to teach or suggest at least that "each of the first and second read data items initiated by the first read operation is read in one clock cycle, and reading the first read data item overlaps with reading the second read data item," as recited in claim 46.

Neither Ryan nor Wright teaches or suggests at least that "the memory circuit is capable to receive a new read or write address in each clock cycle of the clock signal, so that consecutive read and write burst operations are capable to be performed sequentially in any order . . . without any dead clock cycles there between," as recited in claim 54. Indeed, both Ryan and Wright teach away from claim 54.

Ryan describes "a Write Burst followed by a Read Burst" with "a Write mode" selected at "RAS time T0" and "a Switch to Read mode" initiated at "time T7." (Ryan, col. 9, ll. 62-65; col. 10, ll. 1-4.) Fig. 19 shows that the time difference between the read and write bursts is seven clock cycles. Fig. 19 also shows that there are three dead clock cycles, T7, T8, and T9, between the write operation and the read operation. Specifically, "[f]ollowing the read latency period, the first of a burst of four output data elements DOUT n is made available on the data bus 130 at time T10" and "the remaining output data is made available on the data bus, completing the Read Burst with output data DOUT n+3 at time T13." (*Id.* col. 10, ll. 6-11.). Therefore, Ryan fails to teach or suggest at least that "consecutive read and write burst operations are capable to be performed sequentially in any order . . . without any dead clock cycles there between," as recited in claim 54. In fact, Ryan teaches away from claim 54 by teaching the use of the "read latency period" and "one clock cycle external write latency." (*Id.* col. 10, ll. 6-8, 46-48.) Under this teaching, dead cycles are created between or within the read and write burst operations.

Wright does not cure the defects in the teachings of Ryan. Wright describes that "the READ command is issued at time T1 immediately after the WRITE command issued at time T0." (Wright, col. 11, ll. 38-39.) Specifically, "[b]ecause of the read latency of three, the first output data set (DOUT b) [initiated by the READ command issued at time T1] is provided at time T4." (*Id.* ll. 37-40.) Fig. 7 shows that there are two dead clock cycles, T2 and T3, between the write operation and the read operation. Therefore, Wright also fails to teach or suggest at least that "consecutive read and write burst operations are capable to be performed sequentially in any order . . . without any dead clock cycles there between," as recited in claim 54. In fact, Wright teaches away from claim 54 by teaching the use of "a read latency of

three" or "greater than three." (*Id.* col. 11, ll. 30, 45.) Under this teaching, dead cycles are created between or within the read and write burst operations.

Accordingly, even if there is a motivation to combine the teachings of Ryan and Wright, the combination does not teach or suggest all of the limitations of claims 1, 28, 46, and 54.

II. *<u>There is no motivation to combine the teachings of Ryan with those of Wright</u>*

The Examiner suggested that combining the teachings of Ryan with those of Wright would render the claimed invention unpatentable. In particular, the Examiner suggest that "[i]t would have been obvious to one of ordinary skill in the art, having the teachings of Ryan and Wright *et al.* before him at the time the invention was made, to modify the memory system with read and write bursts of Ryan, to include the consecutive initiation of the burst cycles, as in the memory access control system with read and write bursts of Wright *et al.*, in order to improve system throughput by speeding up transition from burst write operations to burst read operations, as taught by Wright *et al.* in column 12, lines 14-20." (Office Action dated June 9, 2003, p. 4-7.) Applicant respectfully submits that there is no motivation to combine or modify the teachings of Ryan with those of Wright in the manner proposed by the Examiner because Ryan's teaching suggests that such modification would defeat the intended purpose of Ryan's teaching.

As noted above, Ryan relates to memory devices having "a Write Burst followed by a Read Burst," with "a Write mode" selected at "RAS time T0" and "a Switch to Read mode" initiated at "time T7." (Ryan, col. 9, ll. 62-65; col. 10, ll. 1-4.) Fig. 19 shows that the time difference between the read and write bursts is seven clock cycles. In particular, Ryan teaches

the use of the "read latency period" and "one clock cycle external write latency." (*Id.* col. 10, ll. 6-8, 46-48.) "If the Switch to Read mode command were instead applied to the memory device at an earlier time, this would interrupt the Write Burst associated with the first applied column address." (*Id.* ll. 11-14.) For example, an earlier Switch to Read mode command in Fig. 20 "interrupts the writing to the memory device of subsequent data in the Write Burst at times T5 and T6." (*Id.* ll. 15-20.)

In contrast, as acknowledged by the Examiner, Wright describes that "the READ command is issued at time T1 immediately after the WRITE command issued at time T0." (Wright, col. 11, ll. 38-39.) Indeed, Wright distinguished their technique over prior art in which "a NOP command must be asserted during the transferring of the last data set of the burst write operation prior to issuing the READ command" and "the NOP command produces a dead cycle or wait cycle between the Write command . . . and the READ command." (*Id.* ll. 15-24.)

Accordingly, were the teachings of Wright, which suggest the technique of following a write command with a read command, used to modify the teachings of Ryan, it would require cutting back the read latency period required by Ryan. Cutting back the required read latency period would "interrupt the Write Burst" and "interrupt[] the writing to the memory device of subsequent data in the Write Burst." (Ryan, col. 10, ll. 11-14, 18-20.) In other words, the proposed modification of the teachings of Ryan with those of Wright would render Ryan unsatisfactory for its intended purpose. Specifically, the proposed combination will prevent completing the data transfers associated with both the read and write burst without interruption. According to the Manual of Patent Examining Procedure §2143.01, "[i]f proposed modification would render the prior art invention being modified unsatisfactory for

its intended purpose, then there is no suggestion or motivation to make the proposed modification." (Citing *In re Gordon* ,733 F.2d 900 (Fed.Cir.1984).)

III. *Hayes does not cure the defects of the teachings of Ryan and Wright*

The Examiner also rejected claims 5-9, 32-36, and 55 under 35 U.S.C. 103(a) as being unpatentable over Ryan, Wright, and Hayes *et al.* (US Patent No. 5,987,570; "Hayes"). As noted above, even were Ryan combined with Wright, the combination does not teach or suggest all the limitations of claims 1, 28, and 54, which claims 5-9, 32-36, and 55 respectively depend from. Additionally, Hayes does not cure the defects of the teachings of Ryan and Wright. Accordingly, claims 1, 28, 46, and 54 and the claims depend from them, including claims 5-9, 32-36, and 55, are patentable over Ryan, Wright, and Hayes.

Hayes relates to "microprocessor bus protocols for cache memories." (Hayes, col. 1, ll. 13-14.) Hayes describes "a read block transaction that hits the cache SRAM array cache 16, followed by a write block transaction that also hits the cache SRAM array cache 16." (*Id.* col. 5, ll. 60-62; Fig. 5.) "[A] read cycle of the SRAM array cache 16 begins [at time 50]" and "[t]he write block transaction begins at time 53." (*Id.* col. 6, ll. 6-7, 24; Fig. 5.) Accordingly, the time difference between initiating a read operation and a write operation is four clock cycles. "Between times 50 and 52, a new address of the read block is loaded into the SRAM array address register" and "[a]t time 53, the first address of the write block is loaded into the cache controller address register." (*Id.* col. 6, 12-13, 31-32.) Fig. 5 shows that, due to the time needed for loading addresses, the data transfers of both the read and write operations do not complete until eleven clock cycles after the read operation begins. In other

words, Fig. 5 shows that eleven clock cycles are needed to complete the data inputs and outputs.

Therefore, Hayes fails to teach or suggest at least that "in two consecutive clock cycles at least a first and a second write data items corresponding to a first write burst operation are capable of being transferred sequentially to the memory circuit via the data bus and at least a first and second read data items corresponding to a first read burst operation are capable of being provided sequentially by the memory circuit via the data bus," as recited in claim 1. Likewise, Hayes fails to teach or suggest at least "(A) initiating a first write burst operation for sequentially transferring at least a first and second write data items to the memory circuit in a first clock cycle; and (B) initiating a first read burst operation for sequentially transferring at least a first and second read data items from the memory circuit in a second clock cycle, wherein the first and second clock cycles are two consecutive clock cycles," as recited in claim 28.

Furthermore, Fig. 5 of Hayes shows, via the "DATA" diagram in the lower part of the figure, that reading one data element does not overlap with reading another data element in any way. Accordingly, Hayes also fails to teach or suggest at least that "each of the first and second read data items initiated by the first read operation is read in one clock cycle, and reading the first read data item overlaps with reading the second read data item," as recited in claim 28.

Fig. 5 of Hayes shows, via the "SRAM CYCLE" diagram at the bottom, that there are three dead clock cycles, 53, 54, and 55, between the read operations and write operations of the SRAM cycle. As a result, Hayes fails to teach or suggest at least that "the memory circuit

is capable to receive a new read or write address in each clock cycle of the clock signal, so that consecutive read and write burst operations are capable to be performed sequentially in any order . . . without any dead clock cycles there between," as recited in claim 54.

For at least the reasons noted above, claims 1, 28, 46, and 54 are allowable over Ryan and Wright. Claims 1, 28, 46, and 54 are also allowable over Ryan, Wright, and Hayes. Claims 2-27 and 57-58, 29-37, 47-53, and 55, which respectively depend from claims 1, 28, 46, and 54, are therefore allowable over Ryan and Wright and over Ryan, Wright, and Hayes for at least the same reasons.

CONCLUSION

Claims 1-58 are pending in this application. Applicant has amended claims 1, 3-5, 28, 40, 46, 48, 49, and 54, canceled claim 56, and added new claims 57 and 58. Claims 1-58, as discussed above, are allowable over the cited references. Accordingly, Applicant respectfully requests that the Examiner reconsider these claims and timely issue a Notice of Allowance for claims 1-58. If the Examiner contemplates a different action, the Examiner is invited to contact the Applicant's representative by phone at 650-849-6622 or by e-mail at gary.edwards@finnegan.com.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

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